In the Claims

Claim 1 (currently amended): A method of forming a plurality of capacitor devices, comprising:

forming conductive capacitor electrode material within openings in a first material comprising silicon and oxygen;

providing a retaining structure in physical contact with at least some of the conductive capacitor electrode material, the retaining structure comprising a dielectric material, the dielectric material of the retaining structure comprising silicon and nitrogen;

removing at least some of the first material while the retaining structure physically contacts the at least some of the conductive capacitor electrode material; ~~and~~

after removing at least some of the first material, incorporating the conductive capacitor electrode material into a plurality of capacitor devices; and

wherein the first material is over the retaining structure.

Claim 2 (cancelled).

Claim 3 (currently amended): The method of claim [[2]] 1 wherein the conductive capacitor electrode material is formed within the openings in the shape of upwardly-opening container structures.

Claim 4 (currently amended): The method of claim [[2]] 1 wherein the conductive capacitor electrode material fills the openings to form conductive pedestals within the openings.

Claim 5 (currently amended): The method of claim [[2]] 1 wherein the first material consists of one or more electrically insulative materials.

Claims 6 and 7 (cancelled).

Claim 8 (currently amended): The method of claim [[2]] 1 wherein the first material comprises one or more of borophosphosilicate glass, spin-on-glass, silicon dioxide, phosphosilicate glass, borosilicate glass, and silicon nitride.

Claim 9 (currently amended): The method of claim [[2]] 1 wherein the retaining structure comprises silicon nitride.

Claim 10 (original): The method of claim 9 wherein the silicon nitride has a thickness of from about 50Å to about 3000Å.

Claim 11 (currently amended): The method of claim [[2]] 1 wherein the first material comprises borophosphosilicate glass and the retaining structure comprises silicon nitride.

Claim 12 (currently amended): ~~The method of claim 2~~ A method of forming a plurality of capacitor devices, comprising:

forming conductive capacitor electrode material within openings in a first material comprising silicon and oxygen;

providing a retaining structure in physical contact with at least some of the conductive capacitor electrode material;

removing at least some of the first material while the retaining structure physically contacts the at least some of the conductive capacitor electrode material;

after removing at least some of the first material, incorporating the conductive capacitor electrode material into a plurality of capacitor devices;

wherein:

the first material comprises borophosphosilicate glass; [[,]] ~~wherein~~

a wet etch is utilized to remove at least some of the first material; [[and]] ~~wherein~~

the retaining structure comprises silicon nitride and a material having increased selectivity to borophosphosilicate glass than silicon nitride during the wet etch.

Claim 13 (original): The method of claim 12 wherein the material having increased selectivity to borophosphosilicate glass than silicon nitride during the wet etch consists essentially of silicon.

Claim 14 (original): The method of claim 12 wherein the material having increased selectivity to borophosphosilicate glass than silicon nitride during the wet etch includes polycrystalline silicon.

Claim 15 (original): The method of claim 14 wherein the polycrystalline silicon is over the silicon nitride.

Claim 16 (original): The method of claim 15 wherein the polycrystalline silicon has a thickness of from about 50Å to about 1000Å.

Claim 17 (original): The method of claim 15 wherein the polycrystalline silicon has a thickness of from about 50Å to about 1000Å; and wherein the silicon nitride has a thickness of from about 50Å to about 3000Å.

Claim 18 (original): The method of claim 14 wherein the polycrystalline silicon is under the silicon nitride.

Claim 19 (original): The method of claim 14 wherein the polycrystalline silicon is over and under the silicon nitride.

Claim 20 (original): The method of claim 19 wherein the polycrystalline silicon below the silicon nitride has a thickness of from about 50Å to about 500Å; wherein the polycrystalline silicon above the silicon nitride has a thickness of from about 50Å to about 500Å; and wherein the silicon nitride has a thickness of from about 50Å to about 1000Å.

Claim 21 (original): The method of claim 14 wherein the polycrystalline silicon entirely surrounds the silicon nitride.

Claim 22 (cancelled).

Claim 23 (currently amended): ~~The method of claim 22~~ A method of forming a plurality of capacitor devices, comprising:

providing a construction comprising a first material over a substrate;

forming a retaining structure over at least a portion of the first material;

forming openings extending into the first material;

forming conductive structures within the openings utilizing a first conductive layer, the conductive structures having outer sidewalls along the first material;

removing at least some of the first material to expose at least portions of the outer sidewalls of the conductive structures, the retaining structure retaining the conductive structures during the removal of the first material;

forming a capacitor dielectric material along the exposed portions of the outer sidewalls;

forming a second conductive layer over the capacitor dielectric material;

wherein the retaining structure is formed before forming the openings, and [[, and]]

wherein the openings extend through the retaining structure.

Claim 24 (currently amended): The method of claim [[22]] 23 wherein the conductive structures are container structures having openings extending therein, and wherein the dielectric material and second conductive layer are formed to extend within the openings that extend into the container structures.

Claim 25 (currently amended): The method of claim [[22]] 23 wherein the conductive structures are pedestals.

Claim 26 (original): The method of claim 23 wherein the openings extend in an array comprising rows and columns; wherein the conductive structures are formed in the array defined by the openings and thus the conductive structures are within an array comprising rows and columns; and wherein the retaining structure is patterned to extend between and connect alternating pairs of the rows of the conductive structure array.

Claim 27 (original): The method of claim 23 wherein the retaining structure is a second retaining structure; and wherein a first retaining structure is formed prior to forming at least some of the first material.

Claim 28 (original): The method of claim 27 wherein a first portion of the first material is formed prior to forming the first retaining structure and a second portion of the first material is formed after forming the first retaining structure; and wherein the first retaining structure is patterned prior to forming the second portion of the first material so that some of the second portion of the first material is formed directly against the first retaining structure and some of the second portion of the first material is formed directly against the first portion of the first material.

Claim 29 (original): The method of claim 23 wherein the retaining structure is a second retaining structure; wherein a first retaining structure is formed prior to forming the first material; and wherein the first material is between the first and second retaining structures.

Claim 30 (cancelled).

Claim 31 (currently amended): ~~The method of claim 22~~ A method of forming a plurality of capacitor devices, comprising:

providing a construction comprising a first material over a substrate;

forming a retaining structure over at least a portion of the first material;

forming openings extending into the first material;

forming conductive structures within the openings utilizing a first conductive layer, the conductive structures having outer sidewalls along the first material;

removing at least some of the first material to expose at least portions of the outer sidewalls of the conductive structures, the retaining structure retaining the conductive structures during the removal of the first material;

forming a capacitor dielectric material along the exposed portions of the outer sidewalls;

forming a second conductive layer over the capacitor dielectric material; and

wherein:

the first material comprises borophosphosilicate glass; ~~wherein~~

an isotropic etch is utilized to remove at least some of the first material; and [[, and]] ~~wherein~~

the retaining structure comprises silicon nitride and a material having increased selectivity to borophosphosilicate glass than silicon nitride during the isotropic etch.

Claim 32 (original): The method of claim 31 wherein the material having increased selectivity to borophosphosilicate glass than silicon nitride during the isotropic etch consists essentially of silicon.

Claim 33 (original): The method of claim 31 wherein the material having increased selectivity to borophosphosilicate glass than silicon nitride during the isotropic etch includes polycrystalline silicon.

Claim 34 (original): The method of claim 33 wherein the polycrystalline silicon is over the silicon nitride.

Claim 35 (original): The method of claim 33 wherein the polycrystalline silicon is under the silicon nitride.

Claim 36 (original): The method of claim 33 wherein the polycrystalline silicon is over and under the silicon nitride.

Claim 37 (original): The method of claim 33 wherein the polycrystalline silicon entirely surrounds the silicon nitride.

Claim 38 (currently amended): The method of claim [[22]] 33 further comprising removing the retaining structure from over the first material after forming the second conductive layer.

Claim 39 (original): A method of forming a plurality of capacitor devices, comprising:

providing a construction comprising a first material over a substrate;

forming openings extending into the first material; the openings extending in an array comprising rows and columns;

forming a first conductive layer within the openings, the first conductive layer within the openings forming container structures having outer sidewalls along the first material wherein the container structures are formed in the array defined by the openings and thus the container structures are within an array comprising rows and columns;

providing a retaining structure which extends between and connects alternating pairs of the rows of the container structure array, the retaining structure being directly against the first conductive layer of the container structures;

removing at least some of the first material to expose at least portions of the outer sidewalls of the container structures, the retaining structure retaining the container structures during the removal of the first material;

forming a capacitor dielectric material along the exposed portions of the outer sidewalls and within the container structures; and

forming a second conductive layer over the capacitor dielectric material.

Claim 40 (original): The method of claim 39 wherein the retaining structure is beneath the first material.

Claim 41 (original): The method of claim 39 wherein the retaining structure is over the first material.

Claim 42 (original): The method of claim 41 wherein the retaining structure is a second retaining structure; and wherein a first retaining structure is beneath at least some of the first material.

Claim 43 (original): The method of claim 39 wherein the first material comprises one or more of borophosphosilicate glass, spin-on-glass, silicon dioxide, phosphosilicate glass, borosilicate glass, and silicon nitride.

Claim 44 (original): The method of claim 39 wherein the retaining structure comprises silicon nitride.

Claim 45 (original): The method of claim 44 wherein the silicon nitride has a thickness of from about 50Å to about 3000Å.

Claim 46 (original): The method of claim 39 wherein the first material comprises borophosphosilicate glass and the retaining structure comprises silicon nitride.

Claim 47 (original): The method of claim 39 wherein the first material comprises borophosphosilicate glass, wherein a wet etch is utilized to remove at least some of the first material; and wherein the retaining structure comprises silicon nitride and a material having increased selectivity to borophosphosilicate glass than silicon nitride during the wet etch.

Claim 48 (original): The method of claim 47 wherein the material having increased selectivity to borophosphosilicate glass than silicon nitride during the wet etch is a silicon-containing material.

Claim 49 (original): The method of claim 48 wherein the silicon-containing material is over the silicon nitride.

Claim 50 (original): The method of claim 49 wherein the silicon-containing material has a thickness of from about 50Å to about 10000Å.

Claim 51 (original): The method of claim 49 wherein the silicon-containing material has a thickness of from about 50Å to about 1000Å; and wherein the silicon nitride has a thickness of from about 50Å to about 3000Å.

Claim 52 (original): The method of claim 48 wherein the silicon-containing material is under the silicon nitride.

Claim 53 (original): The method of claim 48 wherein the silicon-containing material is over and under the silicon nitride.

Claim 54 (original): The method of claim 53 wherein the silicon-containing material below the silicon nitride has a thickness of from about 50Å to about 500Å; wherein the silicon-containing material above the silicon nitride has a thickness of from about 50Å to about 500Å; and wherein the silicon nitride has a thickness of from about 50Å to about 1000Å.

Claim 55 (original): The method of claim 48 wherein the silicon-containing material entirely surrounds the silicon nitride.

Claim 56 (original): A method of forming a plurality of capacitor devices, comprising:

providing a construction comprising a memory array region, a region other than the memory array region and a location between the memory array region and said other region;

forming a first material extending over the memory array region, over said other region, and over the location between the memory array region and said other region;

forming a second material over at least a portion of the first material that is over the memory array region and over an entirety of the first material that is over said other region;

forming openings extending into the first material over the memory array region and forming a trench within the first material over the location between the memory array region and said other region;

forming a first conductive layer within the openings and within the trench, the first conductive layer within the openings forming container structures having outer sidewalls along the first material;

after forming the first conductive layer and the second material, removing at least some of the first material to expose at least portions of the outer sidewalls of the container structures;

forming a capacitor dielectric material along the exposed portions of the outer sidewalls and within the container structures; and

forming a second conductive layer over the capacitor dielectric material.

Claim 57 (original): The method of claim 56 wherein the second material comprises silicon nitride.

Claim 58 (original): The method of claim 57 wherein the second conductive layer and the dielectric material are formed over the second material.

Claim 59 (original): The method of claim 56 wherein the first material comprises borophosphosilicate glass; wherein an isotropic etch is utilized to remove the at least some of the first material; wherein the second material is incorporated into a retaining structure comprising the second material and a third material; wherein the second material comprises silicon nitride; and wherein the third material has increased selectivity to borophosphosilicate glass than does silicon nitride during the isotropic etch.

Claim 60 (original): The method of claim 59 wherein the third material comprises one or both of amorphous silicon and polycrystalline silicon.

Claim 61 (original): The method of claim 59 wherein the third material is over the silicon nitride.

Claim 62 (original): The method of claim 59 wherein the third material is under the silicon nitride.

Claim 63 (original): The method of claim 59 wherein the third material is over and under the silicon nitride.

Claim 64 (original): The method of claim 56 wherein the first conductive layer comprises titanium nitride.

Claim 65 (original): A semiconductor construction, comprising:

a substrate having a memory array region defined therein together with a region other than the memory array region and a location between the memory array region and said other region, said memory array region having a lateral periphery defined to entirely laterally surround the memory array region;

an electrically insulative material over said other region, the electrically insulative material having a lateral sidewall extending around the lateral periphery of the memory array region; and

an electrically conductive liner along the sidewall of the material; the electrically conductive liner laterally surrounding the lateral periphery of the memory array region.

Claim 66 (original): The construction of claim 65 further comprising a silicon-nitride containing material over an entirety of said other region and in direct physical contact with the electrically conductive liner.

Claim 67 (original): The construction of claim 65 wherein said electrically insulative material comprises BPSG, and wherein the silicon nitride-containing material is over the electrically insulative material.

Claim 68 (original): The construction of claim 65 wherein the electrically conductive liner comprises titanium nitride.

Claim 69 (original): The construction of claim 65 wherein the electrically conductive liner consists essentially of titanium nitride.

Claim 70 (original): The construction of claim 65 wherein the electrically conductive liner consists of titanium nitride.

Claim 71 (original): The construction of claim 65 wherein the electrically conductive liner is part of a trough; the trough having first sidewall corresponding to the electrically conductive liner and a second sidewall spaced from the first sidewall.

Claim 72 (original): The construction of claim 71 wherein the second sidewall of the trough has an outer surface facing the memory array region and an inner surface facing the first sidewall; the construction further comprising a silicon nitride-containing layer directly against the outer surface of the second sidewall of the trough and extending toward the memory array region from the outer surface of the second sidewall of the trough.

Claim 73 (original): The construction of claim 72 further comprising a plurality of capacitor constructions over the memory array region; the capacitor constructions extending in an array comprising rows and columns; the capacitor constructions comprising storage nodes which extend in the rows and columns of the array; and wherein the silicon nitride-containing layer extends between and connects alternating pairs of the rows of storage nodes of the array.

Claim 74 (original): The construction of claim 65 further comprising a lateral periphery defined to entirely laterally surround said other region, and wherein the electrically conductive liner laterally surrounds the lateral periphery of said other region.

Claim 75 (original): The construction of claim 74 wherein the electrically conductive liner comprises titanium nitride.

Claim 76 (original): The construction of claim 74 wherein the electrically conductive liner consists essentially of titanium nitride.

Claim 77 (original): The construction of claim 74 wherein the electrically conductive liner consists of titanium nitride.

Claim 78 (original): The construction of claim 74 wherein the electrically conductive liner is part of a trough; the trough having first sidewall corresponding to the electrically conductive liner and a second sidewall spaced from the first sidewall.

Claim 79 (original): A semiconductor construction, comprising:

a substrate having a memory array region defined therein together with a region other than the memory array region and a location between the memory array region and said other region;

a plurality of container structures across the memory array region; the container structures being electrically conductive and comprising inner sidewalls within the container structures and outer sidewalls in opposing relation to the inner sidewalls;

an electrically insulative material over said other region, the electrically insulative material having a lateral sidewall;

an electrically conductive liner along the sidewall of the material;

a capacitor dielectric material along the inner and outer sidewalls of the container structures; and

a second conductive layer over the capacitor dielectric material; the container structures, dielectric material and second conductive material together being incorporated into a plurality of capacitor constructions.

Claim 80 (original): The construction of claim 79 wherein the memory array region has a lateral periphery defined to entirely laterally surround the memory array region; and wherein the electrically conductive liner laterally surrounds an entirety of the lateral periphery of the memory array region.

Claim 81 (original): The construction of claim 79 further comprising a silicon-nitride containing material over an entirety of said other region and in direct physical contact with the electrically conductive liner.

Claim 82 (original): The construction of claim 79 wherein said electrically insulative material comprises BPSG, and wherein the silicon nitride-containing material is over the electrically insulative material.

Claim 83 (original): The construction of claim 79 wherein the electrically conductive liner and the capacitor containers comprise titanium nitride.

Claim 84 (original): The construction of claim 79 wherein the electrically conductive liner comprises titanium nitride.

Claim 85 (original): The construction of claim 79 wherein the electrically conductive liner consists essentially of titanium nitride.

Claim 86 (original): The construction of claim 79 wherein the electrically conductive liner consists of titanium nitride.

Claim 87 (original): The construction of claim 79 wherein the electrically conductive liner is part of a trough.

Claim 88 (original): The construction of claim 87 wherein the trough has first sidewall corresponding to the electrically conductive liner and a second sidewall spaced from the first sidewall; the second sidewall having an outer surface facing the memory array region and an inner surface facing the first sidewall; the construction further comprising a silicon nitride-containing layer directly against the outer surface of the second sidewall of the trough and extending toward the memory array region from the outer surface of the second sidewall of the trough.

Claim 89 (original): The construction of claim 88 wherein the container structures extend in an array comprising rows and columns; and wherein the silicon nitride-containing layer extends between and connects alternating pairs of the rows of the container structure array.

Claim 90 (original): The construction of claim 88 further comprising at least one layer consisting essentially of silicon directly against the silicon nitride-containing layer.

Claim 91 (original): The construction of claim 88 further comprising:

a first layer consisting essentially of silicon over and directly against the silicon nitride-containing layer; and

a second layer consisting essentially of silicon under and directly against the silicon nitride-containing layer.

REMARKS

Claims 2, 6, 7, 22 and 30 are canceled; claims 1, 3-5, 8, 9, 11, 12, 23-25, 31 and 38 are amended; and claims 1, 3-5, 8-21, 23-29 and 31-91 are pending in the application.

The specification is amended to correct several minor errors, and also to indicate that the present application is a continuation-in-part of U.S. Pat. Application Serial No. 10/656,732. Submitted herewith is a new declaration of the inventors indicating that the present application is a continuation-in-part of U.S. Pat. Application Serial No. 10/656,732. Applicant believes that no fee is due for including the claim to benefit of the earlier filing date of application 10/656,732 in the present application at the present time under 37 C.F.R. §1.78(a)(2)(ii) in that the claim for benefit of the earlier filing date is being submitted within16 months of the September 4, 2003 filing of the priority application 10/656,732.

The drawings are amended to correct several minor errors. Specifically, drawing sheets 6 and 10-12 have been amended. The amendments are shown in annotated sheets provided herewith, and also provided herewith are replacement sheets which Applicant respectfully requests be entered in place of the originally-submitted sheets 6 and 10-12.

Applicant respectfully requests entry of the amendments submitted herewith, and examination of the pending claims.

Respectfully submitted,

Dated: 8/9/04

By: _____
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